



21154 PCI-to-PCI Bridge Evaluation Board

User's Guide

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This document describes the 21154 PCI-to-PCI Bridge Evaluation Board (also referred to as the EB154). The EB154 is an evaluation and development board for systems based on the 21154 PCI-to-PCI Bridge chip (the 21154).

The 21154 is a second-generation PCI-to-PCI bridge and is fully compliant with the electrical and protocol requirements of the *PCI Local Bus Specification*, Revision 2.2, and the *PCI-to-PCI Bridge Architecture Specification* Revision 1.0. The 21154 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions. The 21154 has separate posted write, read data, and delayed transaction queues with significantly more buffering capability than first-generation bridges.

For detailed information about the 21154, refer to the *21154 PCI-to-PCI Bridge Data Sheet*.

1.1 Overview

The EB154 is a universal PCI expansion board that is used to evaluate the operation of the 21154 in various configurations, and with a variety of PCI devices. The EB154 can be used to perform the following functions:

- Develop initialization code to configure a PCI-to-PCI bridge and the PCI devices behind the bridge
- Evaluate the operation of a PCI-to-PCI bridge with a variety of PCI devices attached to the secondary bus
- Build and evaluate a flexible hierarchy for multiple PCI buses

1.2 Features

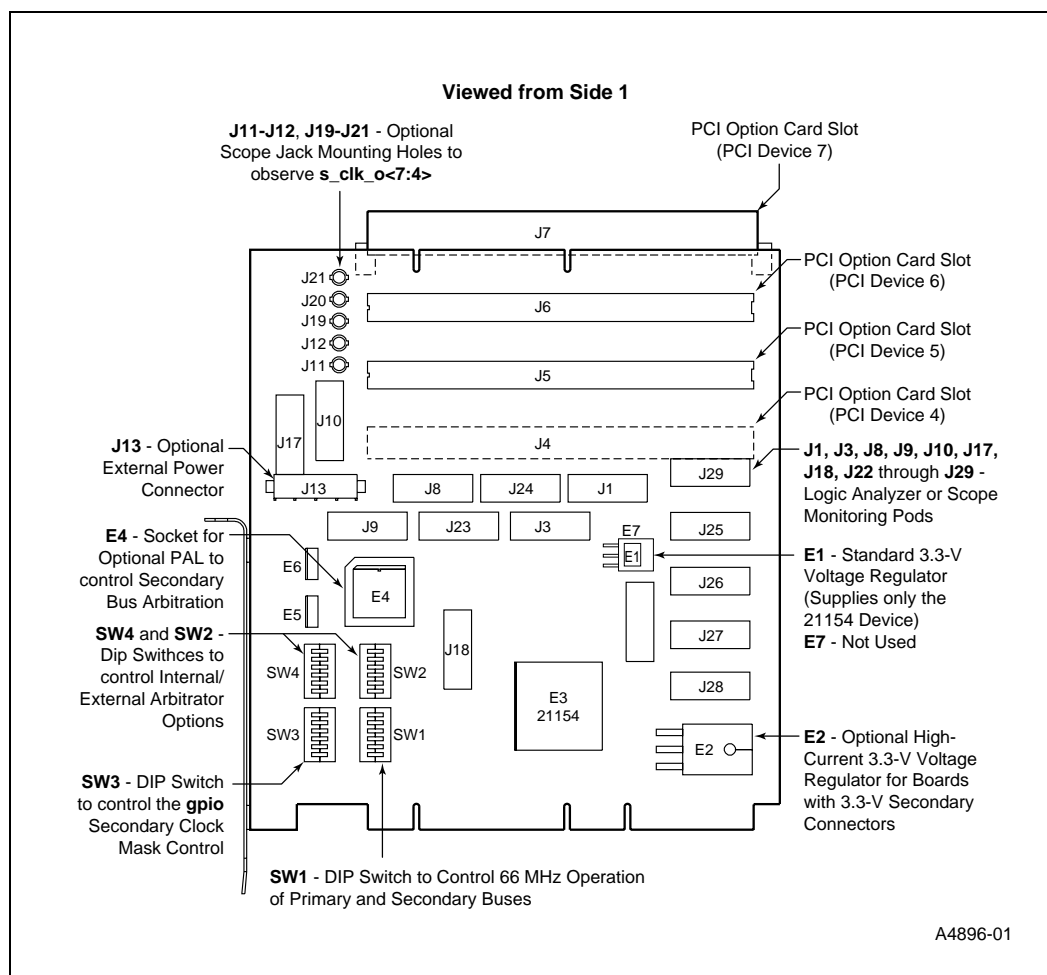
The EB154 has the following features:

- Complies fully with the protocol and electrical standards of the *PCI Local Bus Specification*, Revision 2.2.
- Includes a 21154 PCI-to-PCI Bridge that provides bridging between a 64-bit primary and 64-bit secondary bus.
- Includes a primary PCI bus that plugs into any 5 V or 3.3 V PCI option card slot.
- Provides four secondary 5 V PCI bus option card slots.
- May be built with 3.3 V secondary PCI card slots. If you are interested in this option, call the Information Line.
- Supports an optional external secondary bus arbiter.
- Supports multiple levels of PCI bus hierarchy.

1.3 Major Components

Figure 1-1 shows the major components on the EB154.

Figure 1-1. EB154 Major Components



1.4 DIP Switches

There are four 6-position DIP switches on the EB154. Figure 1-2 shows the locations of the DIP switches, and Table 1-1 describes their operation.

Figure 1-2. EB154 DIP Switches

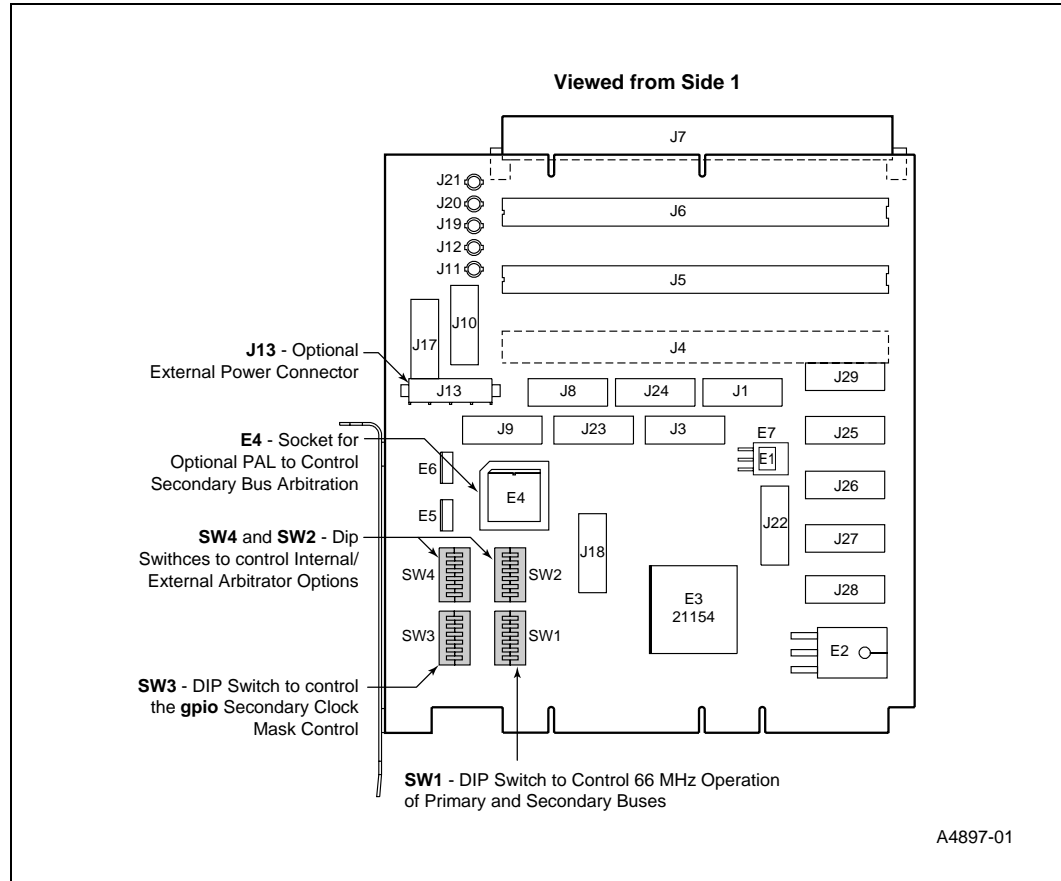


Table 1-1 describes DIP switch operation. Set up DIP switches before powering up the system.

Table 1-1. DIP Switch Operation

DIP Switches	Description
SW1 ¹	Controls 66 MHz operation for primary and secondary buses. Controls MSK_IN . SW1, SW2, and SW3 must be closed for 33 MHz operation.
SW2 ²	Controls the arbiter. For internal arbiter, all positions are closed. For external arbiter, all positions are open.
SW3 ³	Controls the gpio clock mask sequence for secondary clocks s_clk_o<7:4> . For normal operation, all positions are open. This disables the unused 21154 s_clk_o<7:4> clocks.
SW4 ¹	Controls the arbiter. For internal arbiter, all positions are open For external arbiter, all positions are closed.

1. Table 4-5 provides detailed information about configuring this switch.
2. Table 4-1 and Table 4-2 provide detailed information about configuring this switch.
3. Table 4-2 and Table 4-4 provide detailed information about configuring this switch.

1.5 Optional Jumpers

The EB154 provides optional jumpers as a special feature. The jumpers can be used for debugging and for special evaluation tests.

To improve signal integrity, signal **p_clk** and signals **s_clk<3:0>** are not wired to scope pod positions for the default EB154 build. However, provision has been made in the design for viewing these signals if needed.

Table 1-2 shows the connections required to allow observation of these signals at scope pod connector pins.

Table 1-2. Jumper Connections

Jumper	Description
R33 (0-Ω) resistor	If installed, allows observation of p_clk at J9, pin 15.
R44 (0-Ω) resistor	If installed, allows observation of s_clk_o<0> at J17, pin 7.
JW1-to-JW1	If connected with a wire, allows observation of s_clk_o<1> at J17, pin 5.
JW2-to-JW2	If connected with a wire, allows observation of s_clk_o<2> at J17, pin 3.
JW3-to-JW3	If connected with a wire, allows observation of s_clk_o<3> at J17, pin 1.

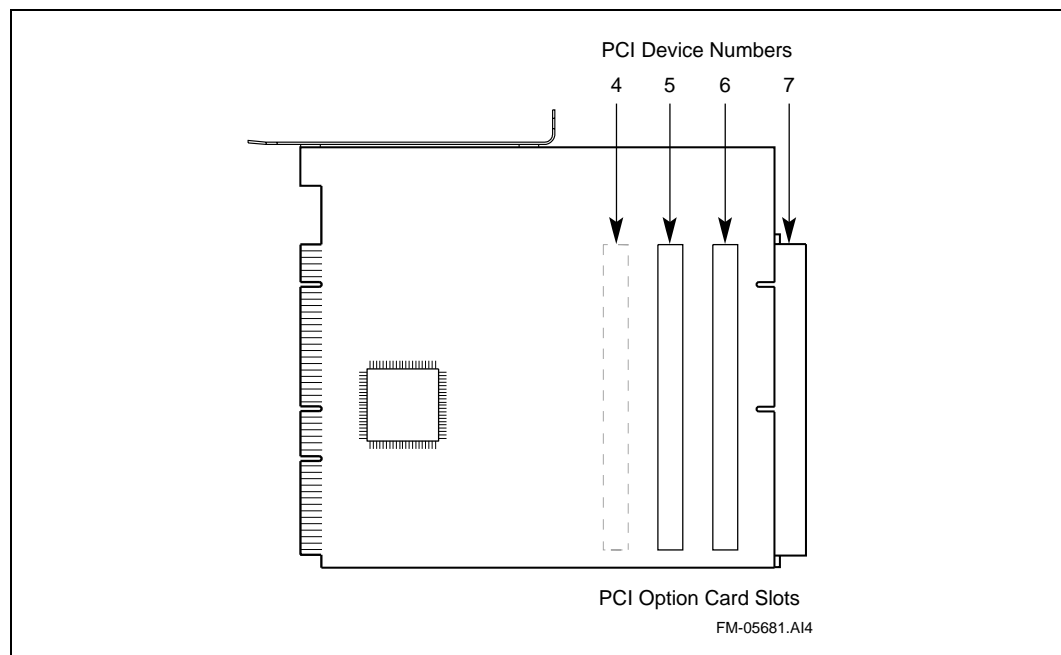
Note: The JW1, JW2, and JW3 holes are located on Side 2 of the EB154. They are labeled in etch. Intel recommends that you use a meter to verify that the correct holes are used for jumper wires before connecting them.

A ground via has been placed to each of the JW1, JW2, and JW3 holes so that a coaxial wire can be used.

1.6 Secondary Slot Numbering and IDSEL Mapping

The PCI secondary bus option card slots are mapped to PCI device numbers 4, 5, 6, and 7 as shown in Figure 1-3. The secondary bus lines **s_ad<20:23>** are used as secondary IDSEL lines.

Figure 1-3. Secondary PCI Slot Numbering



1.7 Typical Configurations

The EB154 supports various PCI configurations with different types of devices. Figure 1-4 through Figure 1-7 show examples of PCI configurations.

The primary bus connector attaches to a PCI slot on the motherboard of the host system or to a secondary PCI bus slot on another EB154. A 5-V or universal PCI option card, or another EB154, can be plugged into any one of the four secondary bus option card slots.

Figure 1-4 shows the EB154 with one secondary bus option card.

Figure 1-4. EB154 with One Secondary Bus Option Card

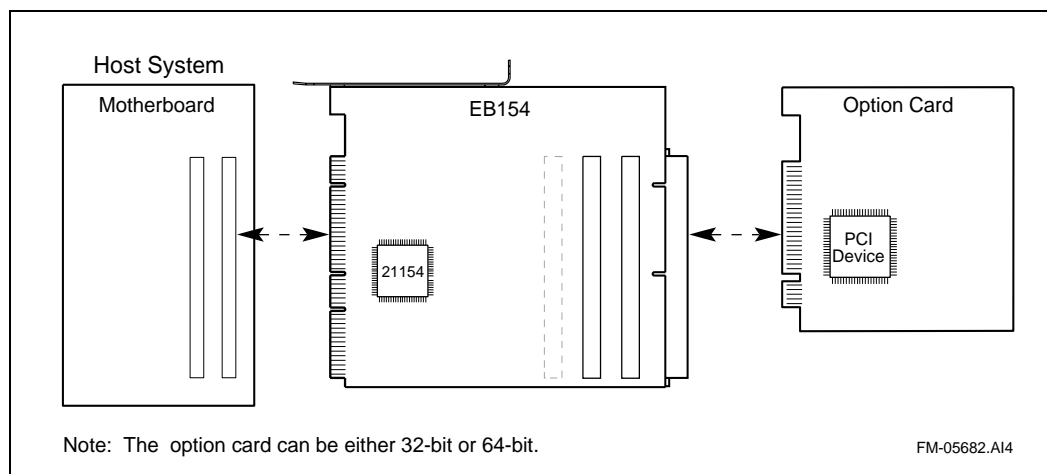


Figure 1-5 shows the EB154 with two secondary bus option cards.

Figure 1-5. EB154 with Two Secondary Bus Option Cards

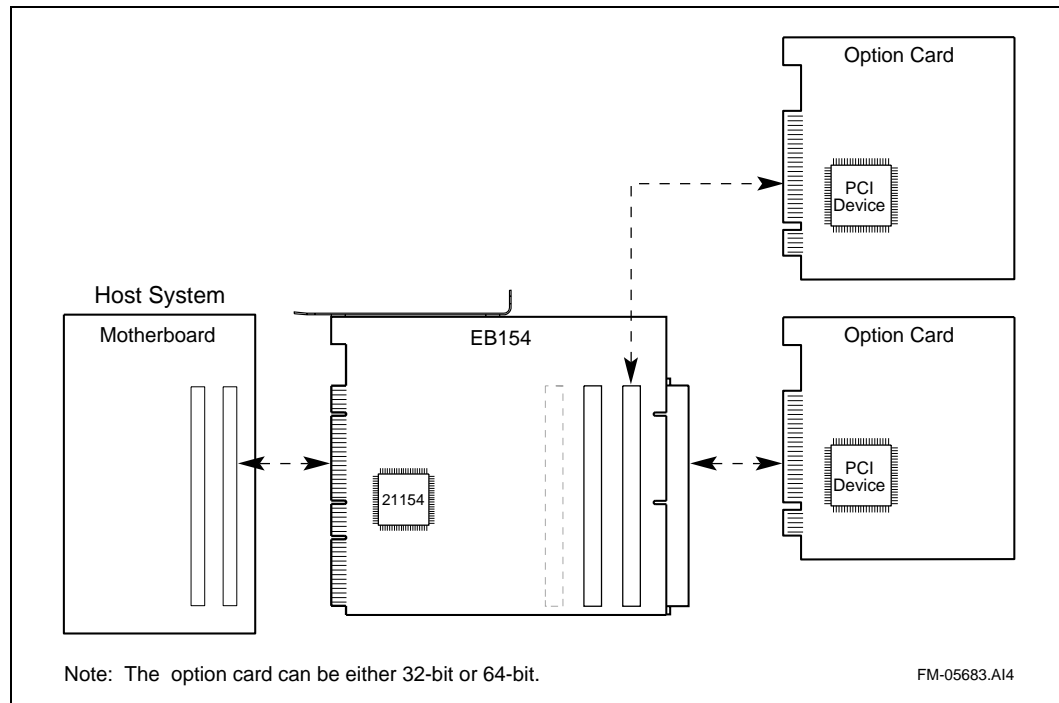


Figure 1-6 shows a tri-level bus with two EB154s.

Figure 1-6. Tri-Level with Two EB154s

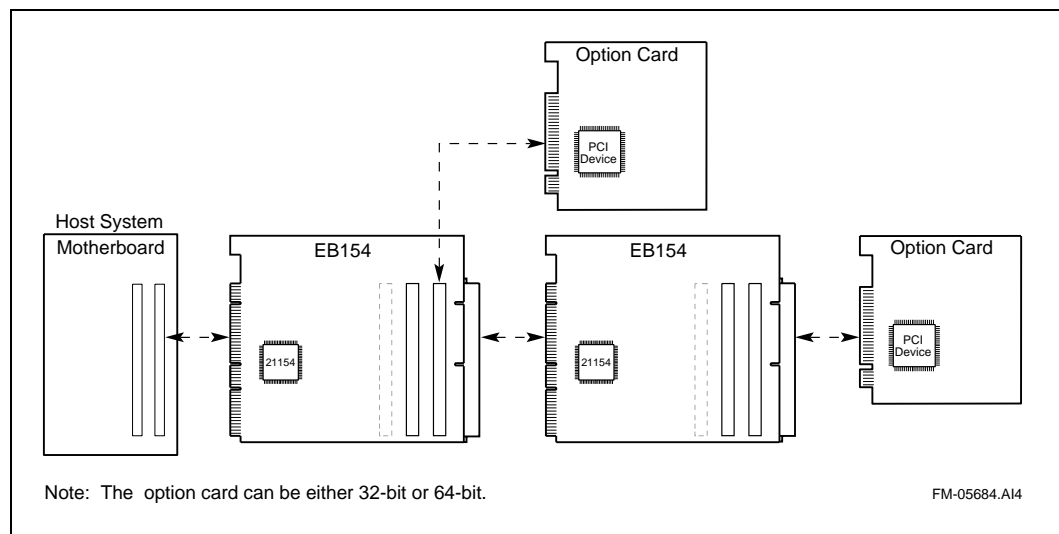
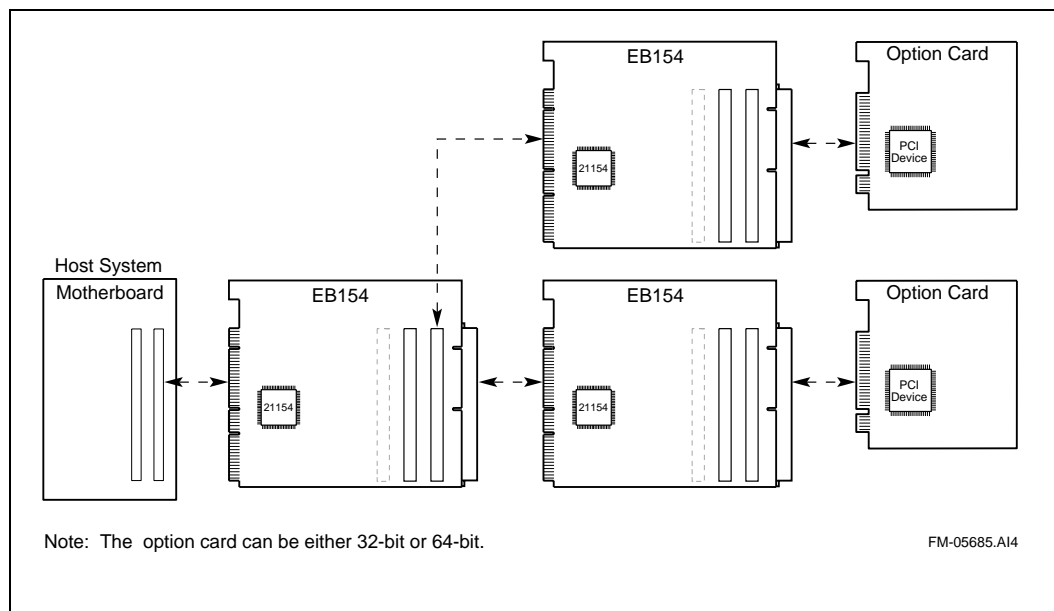


Figure 1-7 shows four PCI buses in a tri-level hierarchy.

Figure 1-7. Four PCI Buses in a Tri-Level Hierarchy

This chapter provides information about the EB154 specifications and the hardware and software requirements for using the EB154. It also describes how to install the EB154.

2.1 Specifications

The physical and power specifications for the EB154 are as follows:

Dimensions:

- Height: 20 cm (7.9 in)
- Width: 17.8 cm (7 in)

Power Requirements:

- DC amps @ 5 V: 2 A (maximum)

2.2 Hardware Requirements

The following equipment is required to use the EB154:

- A computer system equipped with a PCI motherboard
- A PCI expansion slot on the motherboard that is equipped for the 5 V or 3.3 V environment

2.3 Software Requirements

To test the EB154 in x86 DOS or Windows systems, system BIOS must include autoconfiguration code for PCI-to-PCI bridges. If the system BIOS does not include this functionality, contact your BIOS vendor to obtain code with PCI-to-PCI bridge autoconfiguration support.

The EB154 kit provides a DOS utility that can be used to configure the PCI-to-PCI bridge. The diskette included in the EB154 kit contains the DOS utility and a README.TXT file that explains how to use it.

2.4 Installation Procedure

Figure 1-1 illustrates the EB154 and shows the location of components referred to in this section.

Install the EB154 as follows:

1. Power down the host system that will contain the EB154.
2. Place the motherboard with the associated support devices on a bench if mechanical constraints do not allow testing of the EB154 and the expansion slots inside the system box.
3. Configure your system as follows:
 - a. Insert the card edge of the EB154 into a PCI slot.
 - b. Insert a 5 V or universal option PCI card into any or each of the four secondary bus option card slots.
Section 1.7 shows examples of typical PCI configurations.
4. Verify the DIP switch settings for SW1 through SW4 (for normal operation, SW1 positions 1 through 4 and position 6 are closed; position 5 is open).
5. To enable all secondary clocks, open position 4 and close position 5.
6. Power up the system.
7. Verify autoconfiguration of the 21154 and of any devices that are plugged in as follows:
 - a. Verify that system BIOS or firmware detects and configures the PCI devices downstream of the 21154. If system BIOS is not available, use the DOS utility provided with the EB154 kit to configure the devices downstream of the 21154, and verify proper configuration.
 - b. Install device drivers for any PCI devices that are downstream of the 21154, and verify proper configuration of those devices.
8. If desired, monitor bridge PCI control signals by connecting a logic analyzer to pods J1, J3, J8, J9, J10, J17, J18, and J22 through J29.

This chapter describes the way in which interrupts are routed. This information is provided as a reference for designers.

Because a total of 16 interrupts are connected to the secondary bus PCI slots (INTA#, INTB#, INTC#, and INTD# for each slot), and only four interrupts are driven to the card edge, the 16 incoming interrupts must be combined. This ORing of interrupts is performed in accordance with the *PCI-to-PCI Bridge Architecture Specification*.

Table 3-1 shows the ORing of interrupts.

Table 3-1. Interrupt ORing

Device Number	Interrupt Pin on Device	Interrupt Pin on Board Connector
4	INTA# INTB# INTC# INTD#	INTA# INTB# INTC# INTD#
5	INTA# INTB# INTC# I INTD#	INTB# INTC# INTD# INTA#
6	INTA# INTB# INTC# INTD#	INTC# INTD# INTA# INTB#
7	INTA# INTB# INTC# INTD#	INTD# INTA# INTB# INTC#

In accordance with the *PCI Bridge Architecture Specification*, interrupts of the devices on the secondary slots are wire ORed and routed to PCI fingers of the EB154.

Table 3-2 lists the interrupts from the devices on the secondary slots to the interrupts on the EB154 fingers.

Table 3-2. Interrupts from Devices to EB154 Fingers

Interrupts from Devices on Secondary Slots	Interrupts on EB154 Fingers
INTA4 L INTD5 L INTC6 L INTB7 L	INTA L
INTB4 L INTA5 L INTD6 L INTC7 L	INTB L
INTC4 L INTB5 L INTA6 L INTD7 L	INTC L
INTD4 L INTC5 L INTB6 L INTA7 L	INTD L

Note: In the first column of Table 3-2, the number after each interrupt pin is the device number of the devices in the secondary slots. The L indicates that the assertion level is low.

This chapter describes the use of DIP switches to test 21154 secondary bus arbitration and secondary clock control functions.

4.1 Secondary PCI Bus Arbitration

This section describes secondary bus arbitration and the arbitration DIP switches. (For more detailed information about the 21154 arbiter, refer to the *21154 PCI-to-PCI Bridge Data Sheet*.)

The EB154 has two secondary bus arbiter systems:

- An internal arbiter that supports nine external masters in addition to the 21154
- An optional external arbiter implemented in an AMD MACH210A programmable device

The default setting is internal arbitration. The internal 21154 arbiter implements a 2-level programmable rotating mode algorithm. Secondary bus parking is done at the last master to use the bus.

The internal arbiter can be disabled, and an external arbiter can be used instead for secondary bus arbitration. The EB154 provides a socket for an optional PAL (labeled E4 in Figure 4-1) to control secondary bus arbitration. If a different external arbiter is used where parking is done at one of the PCI slots, a PCI device must be installed in that slot. To change the default, configure the secondary bus arbiter system using DIP switches SW2, SW3, and SW4.

Figure 4-1 shows the location of the arbitration DIP switches. Table 4-1 and Table 4-2 describe their operation.

All DIP switch positions assume that the EB154 is positioned with the components facing forward and the card edge facing down.

Figure 4-1. Arbitration DIP Switches

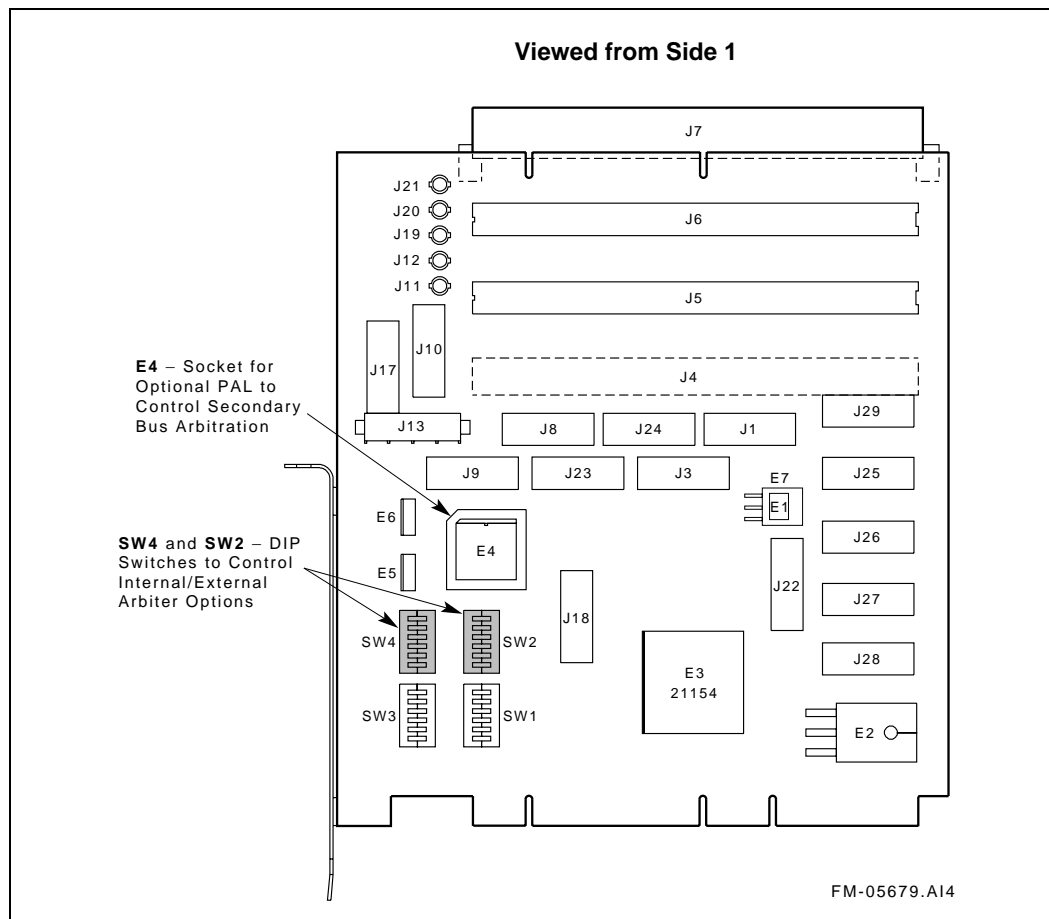


Table 4-1 describes the operation of internal arbitration jumpers.

Table 4-1. Internal Arbitration DIP Switch Positions

DIP Switch	Position	Setting	Description
SW2	1	Closed	When closed, signal s_cfn_l is tied low to enable the internal arbiter.
	2	Closed	When closed, signal s_req_l<0> is tied to one of the secondary PCI connectors for inclusion in the internal arbitration.
	3–6	Closed	When closed, signals s_gnt_l<3:0> are connected from the 21154 to the four secondary PCI connectors for use in the internal arbitration.
SW4	1–5	Open	Disables connection of the s_gnt_l<3:0> and s_req_l<0> signals between the 21154 and the external PAL.

Table 4-2 describes the operation of DIP switches for external arbitration with PAL.

Table 4-2. External PAL Arbitration DIP Switch Positions

DIP Switch	Position	Setting	Description
SW2	1	Open	Enables pull-up for signal s_cfn_l to disable the internal arbiter.
	2	Open	Disables the direct connection of signal s_req_l<0> to a secondary PCI connector.
	3–6	Open	Disables the direct connection of signals s_gnt_l<3:0> to the four secondary PCI connectors.
SW4	1	Closed	Connects signal s_req_l<0> to the external PAL. Because s_cfn is pulled high (SW2, position 1), this signal is used as the s_gnt_l to the 21154 by the external PAL.
	2–5	Closed	Connects signals s_gnt_l<3:0> from the four secondary PCI connectors to the external PAL.
SW3	5	Closed	Enables signal s_clk_o<8> (by means of the gpio mask circuit) for use with the external PAL.

4.2 Secondary Clock Control

This section describes secondary clock control and the secondary clock DIP switch.

The 21154 implements a 4-pin general-purpose I/O gpio interface. During normal operation, the gpio interface is controlled by device-specific configuration registers.

The gpio interface can be used during secondary interface reset to control secondary clocks on the 21154. The 21154 uses the gpio pins and the msk_in signal to input a 16-bit serial data stream. This data stream is shifted into the secondary clock control register and is used for selectively disabling secondary clock outputs. Make sure SW1 switches 4 and 5 are configured correctly, as shown in Table 4-5 on page 4–6.

The gpio clock mask inputs for the *unused* secondary clocks s_clk_o<8:4> are controlled by the secondary clock DIP switch, SW3, as explained in Table 4-4. The gpio clock mask inputs for the *used* secondary clocks s_clk_o<3:0> are controlled by the state of the PCI PRSNT# signals from each of the four secondary PCI slots.

Table 4-3 shows the format of the serial data stream.

Table 4-3. gpio Serial Data Format

Bit	Description	s_clk_o Output
<1:0>	Slot 4 PRSNT#<1:0> or device 0	0
<3:2>	Slot 5 PRSNT#<1:0> or device 1	1
<5:4>	Slot 6 PRSNT#<1:0> or device 2	2
<7:6>	Slot 7 PRSNT#<1:0> or device 3	3
<8>	Device 4 ¹	4
<9>	Device 5 ¹	5
<10>	Device 6 ¹	6
<11>	Device 7 ¹	7
<12>	Device 8 ¹	8
<13>	21154 s_clk input	9
<14>	Reserved	Not applicable
<15>	Reserved	Not applicable

1. Controlled by DIP switch SW3.

For more information about the format of the serial data stream, as presented in Table 4-3, and gpio mask implementation, see Section 10.2 in the *21154 PCI-to-PCI Bridge Data Sheet*.

Figure 4-2 shows the location of the secondary clock DIP switch, and Table 4-4 describes its operation.

Figure 4-2. Secondary Clock DIP Switch

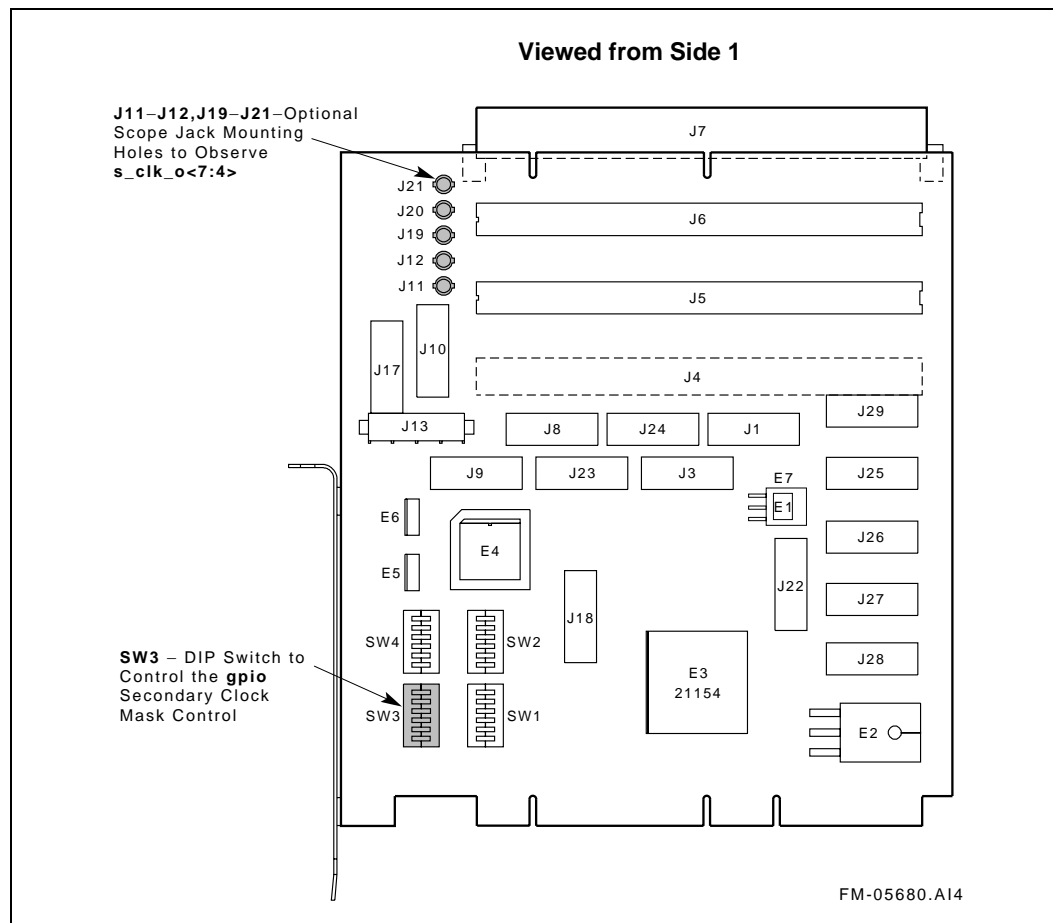


Table 4-4 describes the use of the DIP switch to control secondary clocks.

Table 4-4. Secondary Clock DIP Switch Positions

DIP Switch	Position	Setting	Description
SW3	1–4	Open	For normal operation, the open setting disables the unused 21154 $s_clk_o<7:4>$ clocks.
	1–4	Closed	Positions 1–4 can be closed individually before powering up, to enable 21154 $s_clk_o<7:4>$ clocks selectively for characterization at scope jack locations J12–J15.
	5	Open	Disables $s_clk_o<8>$ when the internal arbiter is used.

4.3 66 MHz Operation

Some versions of the 21154 support 66 MHz operation. All 21154 versions marked 21154-Bx are 66 MHz capable. Versions of the 21154 marked 21154-Ax are not capable of 66 MHz operation.

66 MHz operation is controlled by use of DIP switch SW1. Table 4-5 describes the SW1 switch positions used to control the 21154 operating modes. There are three valid modes of operation:

- 66 Mhz primary bus, 66 MHz secondary bus.
- 66 MHz primary bus, 33 MHz secondary bus.
- 33 MHz primary bus, 33 MHz secondary bus.

Special requirements should be considered for running at 66 MHz. Refer to Section 7.6 of the latest PCI Specification for more information.

- 66 MHz operation requires a 3.3 V signaling environment. s_vio and p_vio signals on the 21154 should be tied appropriately based on the application.
- For motherboard implementations, the 66 MHz slots must be keyed for 3.3 V cards. 5 V add-in cards are not supported.
- 66 MHz add-in cards should provide 3.3 V or universal connectors.

Table 4-5. 66 MHz and msk_in Operation DIP Switch Positions

DIP Switch	Switches	Setting	Description
SW1	1-3	Closed	33 MHz primary bus, 33 MHz secondary bus.
	1-3	Opened	66 MHz primary bus, 66 MHz secondary bus.
	1, 3 2	Opened Closed	66 MHz primary bus, 33 MHz secondary bus.
	5 4	Opened Closed	Enables E5 and E6 to selectively turn on and off S_CLKS 4-8.
	5 4	Closed Open	GND MSK _U disabling E5 and E6 shift registers.

This appendix lists the contents of the 21154 PCI-to-PCI Bridge Evaluation Kit.

The *21154 PCI-to-PCI Bridge Evaluation Kit* contains the following materials:

- A *21154 PCI-to-PCI Bridge Evaluation Board (EB154)*
- A diskette that contains an MS-DOS utility for configuring the EB154
- A documentation package that includes the following:
 - *21154 PCI-to-PCI Bridge Data Sheet*
 - *21154 PCI-to-PCI Bridge Product Brief*
 - *21154 PCI-to-PCI Bridge Configuration Application Note*
 - *21154 PCI-to-PCI Bridge Hardware Implementation Application Note*
 - *21154 PCI-to-PCI Bridge Evaluation Board User's Guide*
 - *21154 PCI Evaluation Board Schematics*
- Level 28 SPICE models for the 21154 and related SPICE documentation are available from the Intel's World Wide Web Internet site at:
<http://www.developer.intel.com/>

